XRM-FCN

High Speed Serial Adaptor Module

User Guide

Version 1.2

Alpha Data
4 West Silvermills Lane
Edinburgh EH3 5BD
UK

Phone: +44 (0) 131 558 2600
Fax: +44 (0) 131 558 2700
Email: support@alphadata.co.uk

Alpha Data
2570 North First Street, Suite 440
San Jose, CA 95131
USA

Phone: (408) 467 5076
Fax: (866) 820 9956
Email: support@alpha-data.com

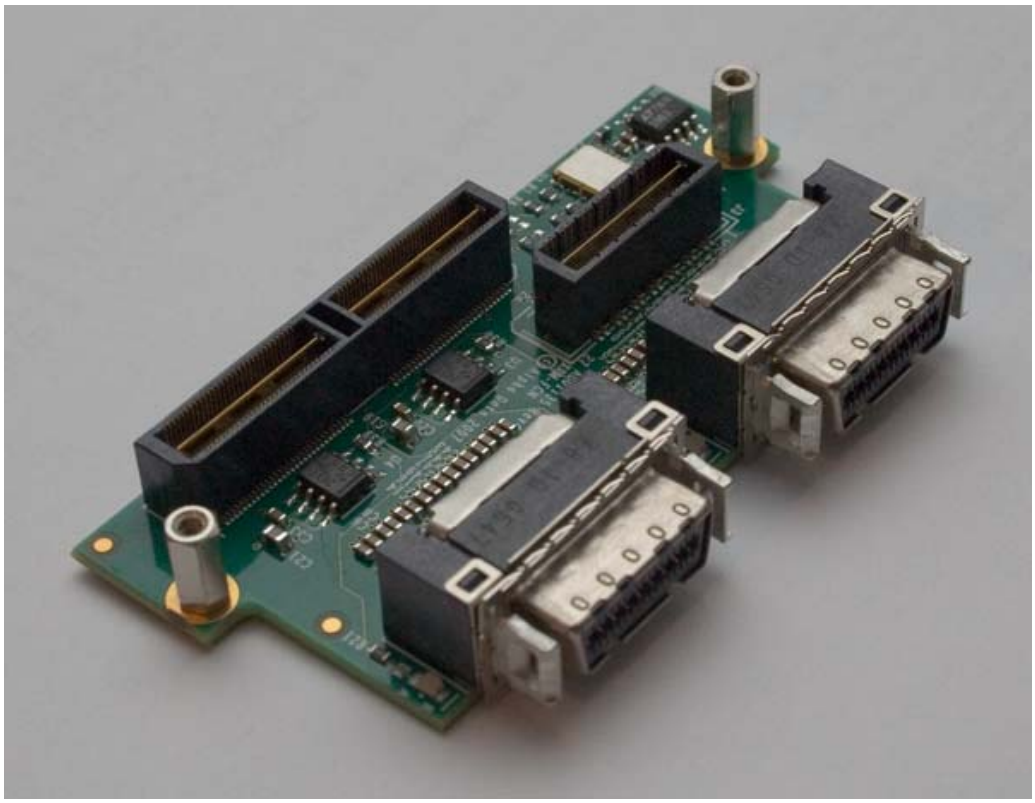
EMI

This equipment generates, uses and can radiate electromagnetic energy. It may cause or be susceptible to electromagnetic interference if not installed and used with adequate EMI protection for specific applications.

Caution

This equipment uses Class 1 Laser devices; such devices are not considered to be hazardous when used for their intended purpose. Use of controls, adjustments or performance of procedures other than those specified herein may result in hazardous laser light exposure.

Table of Contents



1. Introduction

The XRM-FCN is a front-panel adapter card designed for use with Alpha Data's XRC2Pro, XRC4FX, XRC5T1 and XRC5T2 PMC cards. The XRM-FCN provides 8 full duplex channels of high speed serial communications and provides a cost-effective solution to applications requiring high-speed data communications such as Infiniband TA, 10G Ethernet, 4x Fibre Channel and others.

The XRM-FCN allows easy connection of these cards to devices with compatible connectors and signalling standards by means of simple, point-to-point connection schemes implemented using off-the-shelf cable assemblies. Both copper and optical ('CX4') versions of the FCN connector are supported, with full control and fault signalling for each of the optical power connections.

A separate low-jitter oscillator is provided to support high-bit rate applications where the internal clock is unsuitable.

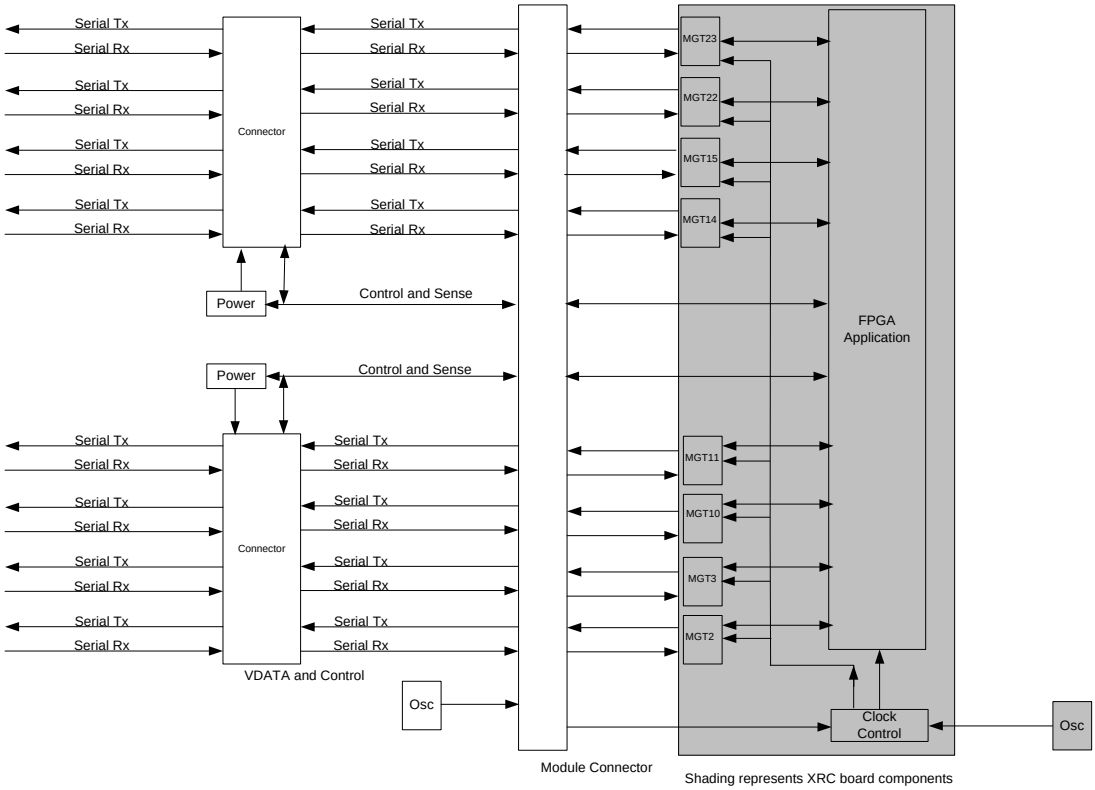


Figure 1 Virtex2 Pro Arrangement

2. Installation

The XRM-FCN is designed to plug in to the front panel connector (SAMTEC QSH series) on XP, XRC4FX and XRC5T. cards. The retaining screws should be tightened to secure the XRM-FCN.

Note: This operation should not be performed while the PMC card is powered up.

2.1. Handling instructions

Observe precautions for preventing damage to components by electrostatic discharge. Personnel handling the board should take SSD precautions. Avoid flexing the board.

2.2. Voltage Settings

This board is a 3V3 only module; users should ensure that the VIO setting on the FPGA card is set to suit this value.

3. Specification

3.1. Mating Cables

3.1.1. Copper

Suitable cables are available from the Fujitsu “microGiGaCN Cable I/O” range of 8-pair cables in a variety of lengths and styles e.g. FCD-ZZ00001.

Molex provide an alternative source with their ‘LaneLink’ cables e.g. 74526 - 1002

3.1.2. Optical

The optical interface is supported on boards from revision 4 on. This uses external modules which plug in to the standard FCN style connector. These modules (e.g. EMCORE QTR3432) convert the electrical signals to optical format. Inter-module connection uses MJ3MM12RPR-10-0 (available from Fiberconnections Inc.) or similar
Please note that these items are not normally supplied by Alpha Data.

3.2. Ordering Information

The oscillator frequencies can be customised to suit applications requiring specific baud rates. Contact the factory for details.

3.3. Example Applications

Dual Infiniband 4x (4 lanes at 2.5Gb/s over copper or optical fibre)
Dual 10Gb/s Ethernet CX4 (4 lanes at 3.125Gb/s over copper or optical fibre)
Dual 10Gb/s FibreChannel (4 lanes at 3.1875Gb/s over copper or optical fibre)
Dual 4 x OC-48 SONET

4. Related Documents

ADM-XRC2ProUser Manual
ADM-XRC4FX User Manual
ADM-XRC5T1 User Manual
ADM-XRC5T2 User Manual

Infiniband™ Architecture Specification, Volume 2 (Release 1.2)

5. Design Examples

Example UCF, HDL files and Application software are available from Alpha Data for purchasers of this card.

5.1. Important Note

Optical modules provide a signal ('sense_l') indicating that they are present; however the presence of optical modules cannot be distinguished from a copper connection by relying on this signal alone.

Whilst the optical module supplies are disabled by default and protected by current limiting, the method shown in the example code should always be used to ensure that supplies do not drive into the short circuit presented when a copper cable is fitted.

Designers should ensure that the FPGA code instantiates a pull-up for the 'fault' and 'op_disable' pins. Power to the modules should then only be enabled when the 'sense_l' line is low **and** 'fault' is high.

Pulling 'op_disable' high ensure no inadvertent emission of radiation.

The 'over_current_l' signal from the supplies are open-collector outputs and should also have a pullup instantiated in the FPGA.

5.2. Pinout

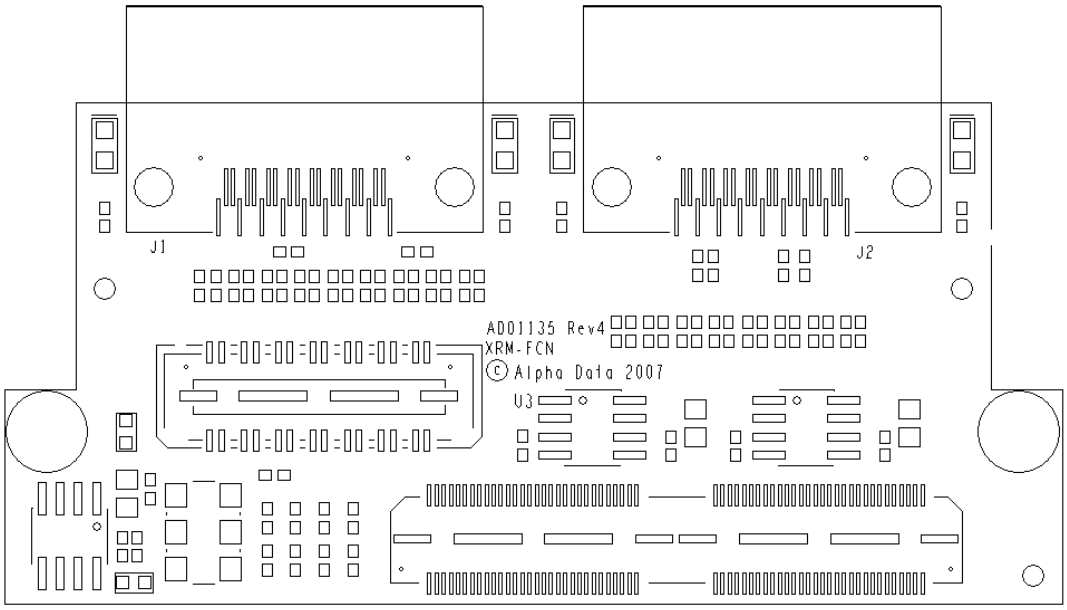
Samtec Pin No.	Signal Name	XRC2Pro	XRC4FX	XRC5T1	XRC5T2	Comment
DP-1	txp<0>	A40	A36	U2	AA2	
DP-3	txn<0>	A41	A37	T2	Y2	
DP-2	rxp<0>	A39	C39	T1	Y1	
DP-4	rxn<0>	A38	D39	R1	W1	
DP-5	txp<1>	A36	A34	M2	T2	
DP-7	txn<1>	A37	A35	N2	U2	
DP-6	rxp<1>	A35	A31	N1	U1	
DP-8	rxn<1>	A34	A32	P1	V1	
DP-9	txp<2>	BB4	P39	L2	R2	
DP-11	txn<2>	BB5	R39	K2	P2	
DP-10	rxp<2>	BB3	U39	K1	P1	
DP-12	rxn<2>	BB2	V39	J1	N1	
DP-13	txp<3>	BB8	M39	F2	K2	
DP-15	txn<3>	BB9	Ne9	G2	L2	
DP-14	rxp<3>	BB7	J39	G1	L1	
DP-16	rxn<3>	BB6	K39	H1	M1	
DP-17	txp<4>	A8	AT39	E2	J2	
DP-19	txn<4>	A9	AU39	D2	H2	
DP-18	rxp<4>	A7	AW37	D1	H1	
DP-20	rxn<4>	A6	AW36	C1	G1	
DP-21	txp<5>	A4	AP39	B4	D2	
DP-23	txn<5>	A5	AR39	B3	E2	
DP-22	rxp<5>	A3	AL39	A3	E1	
DP-24	rxn<5>	A2	AM39	A2	F1	
DP-25	txp<6>	BB36	AW25	B5	B1	
DP-27	txn<6>	BB37	AW24	B6	B2	
DP-26	rxp<6>	BB35	AW22	A6	A2	
DP-28	rxn<6>	BB34	AW21	A7	A3	
117	txp<7>	BB40	AW28	B10	B6	
119	txn<7>	BB41	AW27	B9	B5	
118	rxp<7>	BB39	AW31	A9	A5	
120	rxn<7>	BB38	AW30	A8	A4	
106	osc_enable	L27	AC25	H20	L30	1=Osc enable
73	psu_enable1	H18	D37	AF6	Y40	1=opto power supply on
75	psu_enable2	G18	E37	AE7	W40	1=opto power supply on
90	op_disable1	C19	L26	AH7	T40	1=opto tx disable
92	op_disable2	D19	N35	D11	AF40	1=opto tx disable
76	fault1	M16	E34	V7	W41	1=no opto rx data
84	fault2	G16	J36	U8	AA39	1=no opto rx data
78	sense1_l	K16	D36	W9	K42	0= module present (see 5.1)
86	sense2_l	M17	M32	V9	P40	0= module present (see 5.1)
81	over_current1_l	K19	K34	AJ6	Y42	0= over ccurrent
83	over_current2_l	J19	L34	AJ7	W42	0= over ccurrent
97	brefck_p	G22	T35	K8	AE40	XRC2Pro mgt clock- see note1
99	brefck_n	F22	T34	K9	AD40	XRC2Pro mgt clock- see note1
109	mgt_refck_p	N/A	F39			XRC4/5 mgt clock- see note1
111	mgt_refck_n	N/A	G39			XRC4/5 mgt clock- see note1- see note1
70	atten_led1	C15	F35	Y6	J41	green, 1= on
62	atten_led2	H20	C32	AD7	AA37	green, 1= on

72	status_led1	C14	G35	W6	H41	yellow, 1= on
64	status-led2	J20	C33	AC7	Y37	yellow, 1= on

Notes

1) The on-board ref oscillator can be use to drive the BREFCLK pins (G22,F22) for MGTs on the XRC2PRO. These pins do not drive an MGT reference clock input on XRC4 or XRC5 boards - use pins 109 and 11 instead (configurable by 0R links).
2) Pin numbering and allocation in accordance with Infiniband™ Architecture Specification, Volume 2 section 7.4.3. (Release 1.2)

6. Board Layout



Revision History

Date	Revision	Nature of Change
May-2005	-	Initial draft
Feb-2008		Added documentation for V4 and V5 MGT clock differences, documented optical module additions